International Journal of Mechanical and Production Engineering Research and Development (IJMPERD)
ISSN (P): 2249-6890; ISSN (E): 2249-8001
Vol. 7, Issue 6, Dec 2017, 71-78

DESIGN OF LOW POWER AND AREA EFFICIENT FULL ADDER FOR ALU USING 90NM PROCESS FOR INDUSTRIAL BASED CAD/CAM MANUFACTURING UNITS

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ABSTRACT

The research article shows a high accuracy of full adder with less zone and power utilization. The GDI based full adder wasactualized by utilizing both entryway dispersion through input gate diffusion system and rationale pass transistor that reduces the area and power. To reduce the static power, ultralow control diode was utilized. The leakage current of the diode exists in scope of pA. The experimental work has been done through existing framework like CMOS, CPL and cross breed full adders with a proposed full adder. Every full adder was composed with gpdk 0.90 um in Cadence Virtuoso schematic and simulations were done in a Specter Simulator..

KEYWORDS: CMOS, GDI, Hybrid full adder, CPL

Received: Sep 19, 2017; **Accepted**: Oct 09, 2017; **Published**: Oct 30, 2017; **Paper Id**: IJMPERDDEC20177

Original Article

INTRODUCTION

The adder is an essential building block of numerous computerized circuits like an advanced flag processor (DSP), chip, and furthermore it assumes that the array multiplier plays the vital role in partial product multiplication process. In arithmetic unit binary addition that plays the major role in every arithmetic operation was performed by addition operation. So building and high performance adders would affect the system performance and also reduce the whole power consumption[6]. To improve the whole circuit performance is crucial. The proposed full adder was designed with a minimum number of transistors and it causes the low power consumption and also less area

.REVIEW OF DIFFERENT FULL ADDER TECHNOLOGIES

In the recent years, there are so many logic styles have been proposed to implement 1-bit full adder cells. [1-2]. The full adders are mainly essencially arranged into two types, one is static and another one is dynamic full adders. Static full adders consume less power than the dynamic full adders, because dynamic logic is a clocked logic. For N-input module, static requires 2N transistors and dynamic requires N+2 transistors. It is shown in figure -1. The benefit of utilizing dynamic rationale is speedy exchange and less static power dissipation . Hybrid logic styles can improve high performance. The manufacturing and conventional products cycle used in CAD/CAM are shown figure 2 and 3.

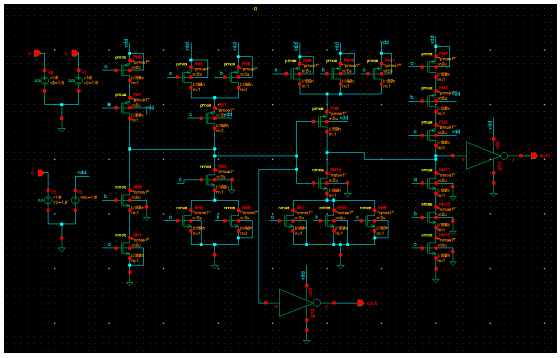

Figure 1: Schematic Diagram of CMOS Full Adder in 90nm Technology using Cadence.

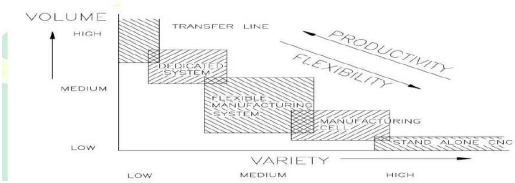

Figure 2: Manufacturing Methods Based on Production Quantity

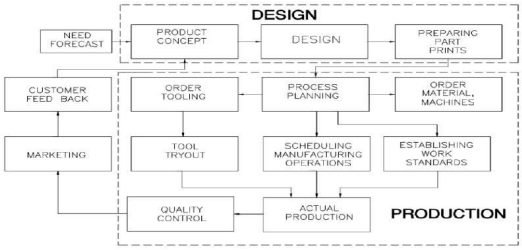

Figure 3: Product Cycle in Conventional Manufacturing Environment

CPL Full Adder

The CPL circuits were designed by using NMOS pass transistor network with CMOS inverters. In the output stage, the CPL differs from pass transistor logic because source terminal of the pass transistor is not connected to either power supply or ground. It should be connected to any one of the input. The block diagram of a full adder which is using CPL as shown in the figure-4. The number of transistors which is required to design CPL full adder is less than the CMOS full adder.

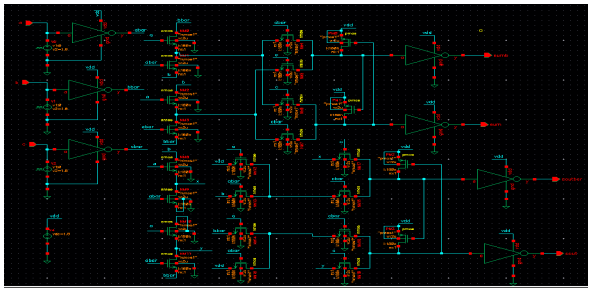

Figure 4: Schematic of CPL Full Adder in 90nm Technology Using Cadence

Hybrid Full Adder

This hybrid full adder contains Semi-XOR and Semi- XNOR [9, 10] gates, instead of normal XOR and XNOR gates, the structures of the Semi-XOR and Semi-XNOR gates, as shown in Figure-3. The output of these gates is same as a normal XOR and XNOR gates, except 11 in Semi- XOR and 00 combinations in Semi-XNOR gates.

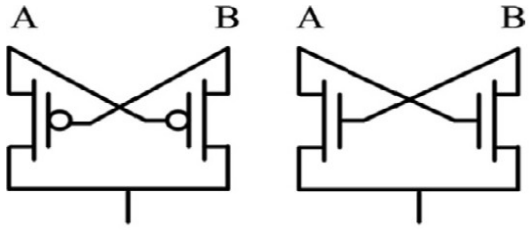

Figure 5 (A): Semi-XOR (B) Semi-XNOR

The truth tables of Semi XOR and Semi XNOR gates, as shown in table 1 (**HZ** is high impedance state)

Table 1: Full adder operation output

A	B	C_{in}	SUM	C_{out}	Semi-XOR	Semi-XNOR
0	0	0	0	0	0	HZ
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	HZ	1
1	0	0	1	0	0	HZ
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	1	HZ	1

For Cout, using Semi XOR-XNOR gates and selector the circuit was designed[9-10]. To prevent the high impedance states (when both inputs are 1s or both 0s), one extra NMOS and PMOS transistor were added. The source of NMOS was connected to Cout, drain to Vdd and gate, to Semi XNOR output and the source of PMOS to Cout, drain to ground and gate to Semi XOR output[6]. To achieve the full swing ULP diode was used. The diode consists of one PMOS and one NMOS transistors, as shown in Figure-6..

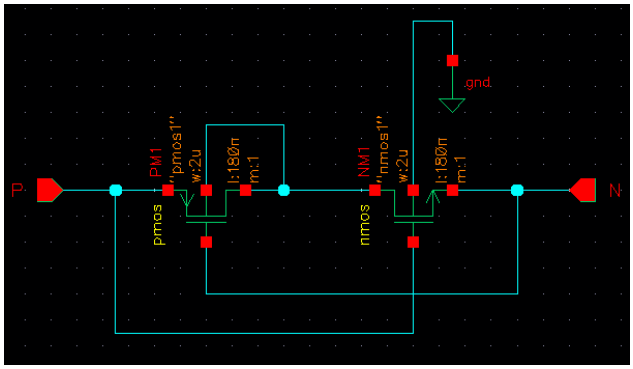

Figure 6: Schematic view of Ultra low power diode

Proposed Full Adder

A new approach to eliminating the use of XOR and XNOR gates, in full adder design is full adder using GDI-MUX and pass transistor. Using GDI-MUX technique AND, OR and multiplexer are implemented, by using this gates and

pass transistor logic a new full adder is implemented, as shown in Figure-8.

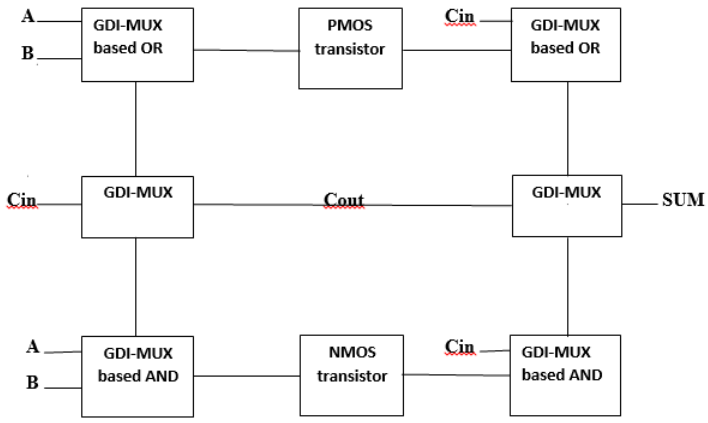

Figure 7: Another Logical Structure for Designing Full Adder

The GDI (Gate Diffusion Input) cell consists of one PMOS and NMOS transistor. Its look like a static CMOS inverter but it differs because the GDI cell [11] has two extra inputs as shown in Figure-9.

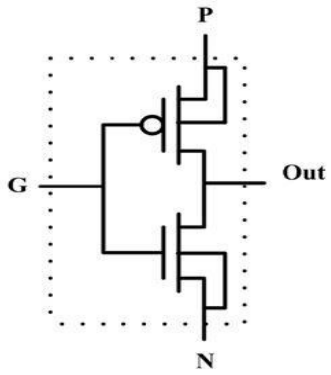

Figure 8: GDI Cell

Those extra two inputs are P (input to source/drain of PMOS) and N (input to source/drain of NMOS). The source terminals of PMOS and NMOS are connected to Vdd and ground. The GDI-MUX based OR gate is modeled by connecting source/drain of NMOS (N input) to Vdd, common gate (G input) to A and P input to B. Similarly AND gate is designed by connecting N input to B, G to A and P input to GND. The basic principle is

For **OR** gate based on truth table

If (A==0)

Y= B;

Else if (A==1)

Y= 1 or Vdd

For **AND** gate based on truth table

If (A==0)

Y= 0 or Gnd;

else if (A==1)

Y= B;

From truth table of a full adder, we can consider that, when Cin = 0, the full adder Cout is equal to A AND B otherwise it is equal to A OR B. By, using multiplexer Cout is selected. As shown in table 3 and 4.

Table 2: OR Gate Operation

Cin	A	B	Cout = A OR B
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 4: AND Gate Operation

Cin	A	B	Cout = A AND B
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

SIMULATION AND RESULTS

Every single full adder was planned and simulated by utilizing a Cadence Virtuoso in 90nm gpdk CMOS innovation. Power dissipation was measured by changing voltage from 1.7 to 2.0 V. The transient response of various full adders as appeared in figure-9, figure-10 and figure-11.

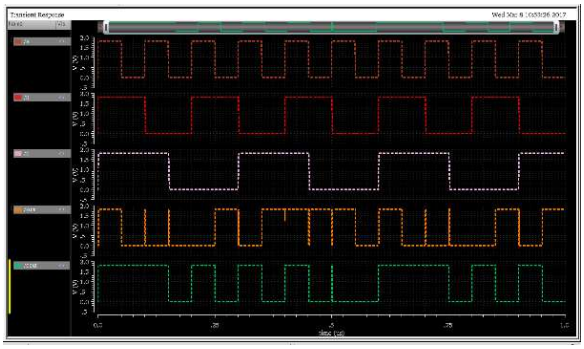

Figure9: CPL full adder transient response using 90nm process

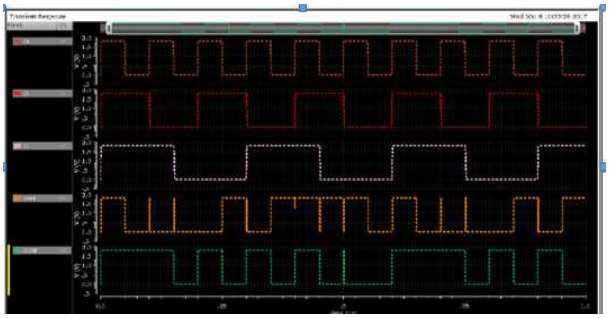

Figure 10: Transient response of proposed full adder using 90nm process flow

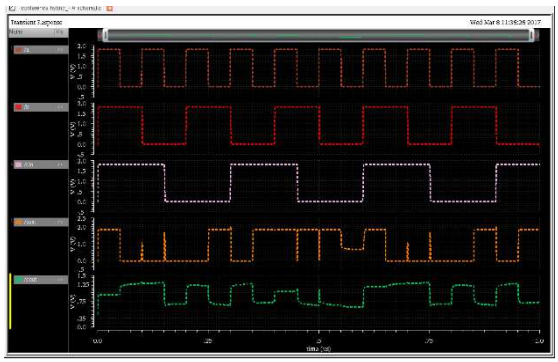

Figure11: Hybrid full adder transient response using 90nm process flow

OBSERVATIONS

Power dissipation is calculated by varying supply voltage from 1.5 to 1.8V as shown in table-5.

Table 4: (power utilization)

Supply Voltage(V)	CMOS (Uw)	CPL (Uw)	Hybrid CMOS (Uw)	Proposed Full Adder (Uw)
1.5	4.55	255.06	2.31	0.404
1.6	5.33	308.33	2.67	0.481
1.7	6.25	366.49	3.07	0.573
1.8	7.26	429.59	3.54	0.678

CONCLUSIONS

Power dissipation was calculated by varying supply voltage from 1.7 to 2.0V as shown in table-4 .Different sorts of full adders were outlined utilizing diverse rationale styles. These CPL and half full adders were contrasted with new proposed full adder. The hybrid and new proposed full adder consumes less number of transistors. As a result the less number of transistors brings out less exchanging movement and range. Power utilization was increased with expanding supply voltage as appeared in table 4.

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